Exploration of Single Spin Logic (SSL) Based Expandable Hardware Design

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Abstract—Expandable Hardware architecture is a hot cake in designing next generation logic circuits to optimize large number of inputs. Classically it maintain higher number of inputs thereby causing excessive power dissipation and this leads to a challenge in exploring consumable expandable hardware. Since the dawn of this decade numerous attempts are made to overcome the power dissipation hindrance. On the other hand, Single Spin Logic(SSL) is an approach that offers low power consumption and no/very low power dissipation, high packing density, high speed like merits to replace the age old CMOS technology. Thus the authors intend to use SSL in designing future expandable hardware. This technical note clearly provides an empirical study of expandable hardware design using SSL.

Index Terms—Single Spin Logic (SSL), Expandable hardware, antiferromagnetic, power dissipation, robustness, not wired, ASIC.

1 Introduction

NOWa day's device miniaturization is a great challenge in VLSI/ULSI circuit design. To accomplish such requirement Carbon Nano Tubes (CNT), Resonant Tunneling Devices (RTD), Rapid Single Flux Quantum (RSFQ) and Quantum Dots (QD) are the few design techniques which are already in use.Before the late 90's the device research emphasized on charge based electron devices but it suffers from leakage power problem which is extremely catasthropic. To overcome this problem a new technology was developed that involves the spin properties of an electro rather the charge. Concurrently it is satisfactorily incorporated in logic designings and give the idea of Single Spin Logic (SSL) [2]. SSL plays a great role in designing NAND gates (H. Agarwal et.al.) [3], Full Adder (SoumitraShukla et.al.) [4], Multiplexer (T.K. Bhattacharyya) [5] and so on.

On the other hand Evolvable Hardware (EHW) [6] is remarkable invention of 21st century where hardware typically grow by themselves based on the operational maneuver. The exquisite proliferation of EHW is that is simply follows the Genetic Algorithm (GA) in logical designing. But to what extend it can prosper is a million dollar question. The reason is that present day EHWs are solely made of CMOS [7] and thus it faces specific stringent. The authors herein after reasonably feels that there is an ample dearth in this research and this is why the others intend to mobilize SSL in designing EHW.

2 SSL Based Logical Invention

In digital electronics AND, OR, NOT gates are the basic gates by which any logical operation can be implemented.A SSL based desining of these basic gates are depicted in fig 1 where green arrows represent the inputs and blue arrows represent the outputs.

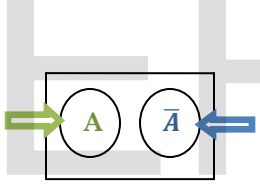

Fig1a: SSL based NOT gate

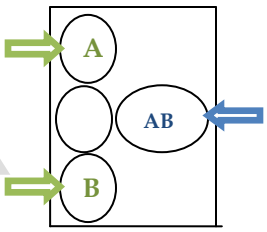

Fig1b: SSL based AND gate

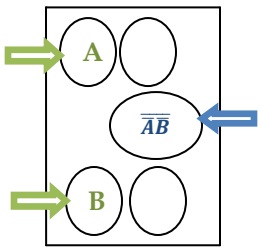

Fig1c: SSL based OR gate

3 Expandable Hardware

EWH is a new and novel idea based on reconfigurable structure of digital logic system. The key to success of evolvable system is that - its function and parameters dynamically changes time to time based on the requirement of the structure. Based on Darwin's theory of evolution and survival of the fittest, EWH is categorized in i) global/local and ii) maximum/minimum entity. Most efficiently they move further from Darwin's theory and settles itself using Self Organizing Migrating Algorithm (SOMA). Although SOMA largely propagates standard GA which represents the basic element as an

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'individual'- i.e. a single solution to the optimized problem. Such identical individuals form a 'population'.

The interconnection between Evolutionary Algorithm (EA) and reconfigurable structure is that EHW follows EA although EHW and evolutionary circuit design which is based on EHW is distinctively different from each other. There are several approaches to implement EWH in combinational logic circuit using stochastic PLDs, FPGAs and advanced processors. But the fragality is that real time implementation of circuit is far lagging because of the physical constrains of CMOS. This type of evolution is comparatively slow and there by insufficiency for exact circuit model is largely ousted. Amid such one can opine that it is elementary but challenging field of research which is not only exciting but also there are few unresolved techniques to improvise EHW in consumable electronics. SSL is likely to be the optimum solution to design EHW of this decade.

4 Architectural View of SSL Based Expandable A/O

To cope up with the spacing limitations herethe authors wouldnot include the basic designing criterions of SSL and only opt to some well known hardware approaches such as a) Expandable 4-wide A/O gate, b) 2-wide 4-input AOI gate, c) 4-wide,2-input AOI gate, d) 4-2-3-2 AOI gate.

The logical representation of SSL made EHW is provided in the following where all inputs and outputs are representated by green and blue lines respectively.

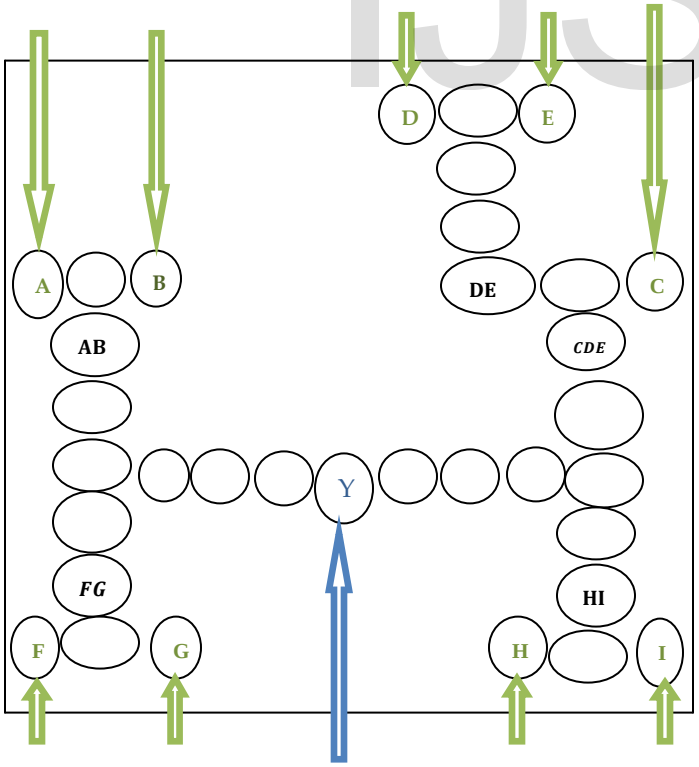

Fig 2a: SSL realization of Expandable 4-wide A/O gate

The spin interaction in fig 2a originates from the A, B, C, D, E, F, G, H, I inputs and the output is the combinational derivation of inputs denoted by Y=AB+CDE+FG+HI.

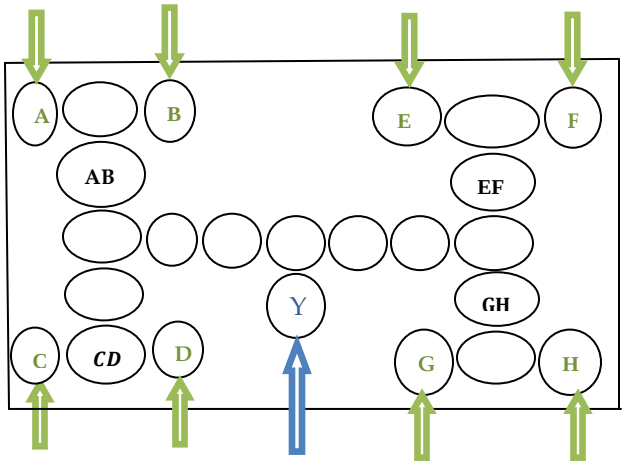

Fig 2b: SSL realization of 2-wide 4-input AOI gate

Fig 2b shows a2-wide 4-input AOI gate can be realiged by spin using inputs A, B, C, D, E, F, G , H and output Y=$\overline{ABCD + EFGH}$

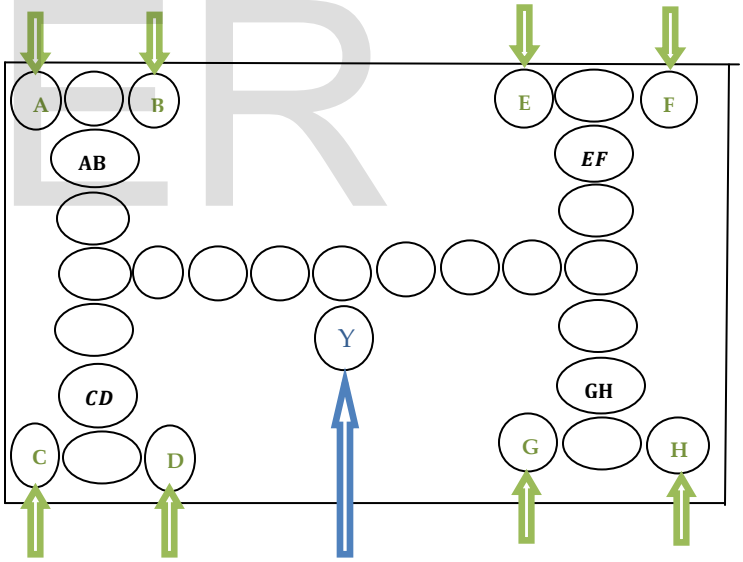

Fig 2c: SSL realization of 4-wide,2-input AOI gate

The spin realization of 4-wide,2-input AOI gate can be made by fig 2c where A, B, C, D, E, F, G, H are the inputs and

Y=$\overline{\boldsymbol{AB + CD + EF + GH}}$ is the output.

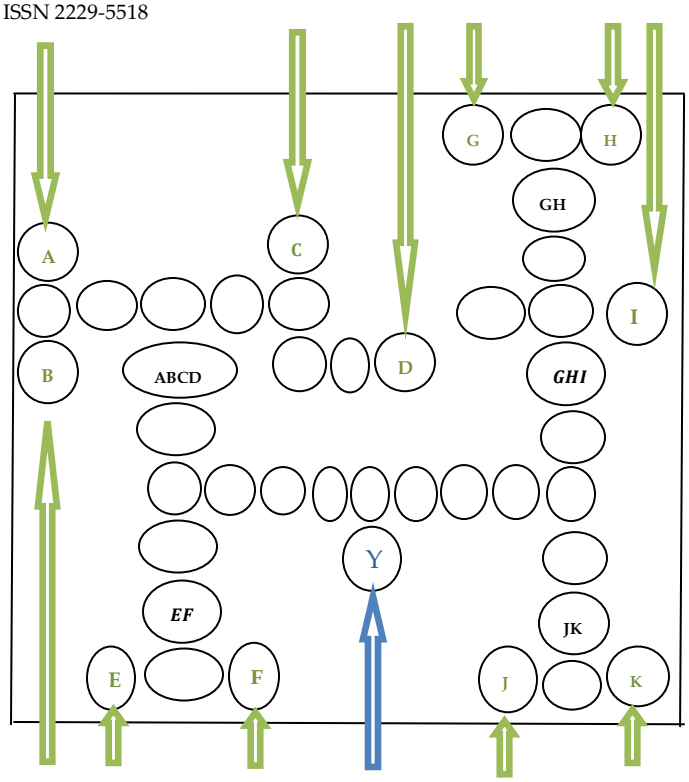

Fig 2d: SSL realization of 4-2-3-2 AOI gate.

A 4-2-3-2 AOI gate where A, B, C, D, E, F, G, H, I, J, K are the inputs and $Y = \overline{ABCD + EF + GHI + JK}$ is output, can be designed by using fig 2d.

From the all above designes we can visualize that no wiring is required for spin realization which is very advantageous over CMOS technology. Due to the wireless designing SSL based design resemble very low propagation delay, and also offer high electronic speed. Additionally, in conventional designing process to change the polarity of electron wenedd to change a lot of circuitwiring connectionwhere as by using SSL this can be achived only by changing the spin direction; thus it is much faster than any other technology.

5 Conclusion

From the above discussion it is very clear that SSL based desing presents light weight, low cost, long duration battery operation likemeris which make it undoubtlyacceptable in logic designing and also in EHW. Moreover, for EHW designing the customary is to realize circuits that donot require many refreshings. SSL obviously diminish the refreshing requirements. All such potentials are to be integrated in future EHWs as SSL is anticipated to be the only composite material of EHWs. Amid such, the authors truly adhere to the SSL technology to build the future EHWs.

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References

[1] Marc Cahay, SupriyoBandyopadhyay, "An electron's spin---Part I", IEEE Potentials,Vol:28, Issue: 3,pp 31-35, 2009.

[2] Subir Kumar Sarkar et.al., "SPINTRONICS DEVICE BASED POWER EFFICIENT VLSI CHIP DESIGN FOR UNIVERSAL CODE CONVERTER", Canadian Journal of pure & applied science, SENRA Academic Publishers, Burnaby, British Columbia,Vol.2,No.3,pp 595-600,2008,IISN: 1715-9997.

[3] H. Agarwal et.al.,"Single spin universal Boolean logic gates", IOP Publishing and Deutsche PhysikalischeGesellschaft, New Journal of Physics, volume 10,January 2008.

[4] Soumitra Shukla et.al, "1-BIT FULL ADDER IMPLEMENTATION USING SINGLE SPINLOGIC PARADIGM", World Scientific Journal, Spin, Vol:10. 1142/S2010324712500129.

[5] T.K. Bhattacharyyaet.al., "Single-Spin implementation of a multiplexer", Elsevier Journal, Physica E 41(2009) 1184-1186.

[6] T. Higuchi, M. Iwata, I. Kajitani, H. Iba, Y. Hirao, B. Manderick, and T. Furuya. Evolvablehardware and its applications to pattern recognition and fault-tolerant systems. In E. Sanchezand M. Tomassini, editors, Towards Evolvable Hardware: The evolutionary Engineering Approach, Vol: 1062 of Lecture Notes in Computer Science, pages 118.135. Springer-Verlag,1996

[7] Dr. JayantaGopeet.al.,"Hybrid CMOS-SET Decision Making Nano IC: A Case Study" , International Journal of Science, Engineering and Technology Research (IJSETR), Vol 4, Issue 6, pp 1768-1772, June 2015